What is claimed is:

1. A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

    doping a first region of a semiconductor substrate;

    incising the substrate to provide an array of edges having substantially vertical edge surfaces, pairs of the edge surfaces facing one another and spaced apart a distance equal to one half of a pitch of the array of edges;

    doping second regions between the pairs of edge surfaces;

    disposing respective structures each providing an electronic memory function on at least some respective ones of the edge surfaces; and

    establishing electrical contacts to the first and second regions.

2. The method of claim 1, wherein disposing comprises:

    forming ONO structures on at least some respective ones of the edge surfaces; and

    creating respective gates on the ONO structures.

3. The method of claim 1, wherein disposing comprises:

    forming ONO structures on at least some respective ones of the edge surfaces; and

    creating respective gates on the ONO structures, wherein forming ONO structures comprises:

    growing silicon dioxide from silicon comprising the edge surfaces;

    forming a silicon nitride layer on the silicon dioxide; and

    forming silicon dioxide on the silicon nitride.

4. The method of claim 1, wherein disposing comprises forming respective polysilicon gates on respective ones of the surface edges.

5. The method of claim 1, wherein disposing comprises:

    forming a first gate dielectric on the surface edge;

    forming a floating gate on the first gate dielectric;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

6.   The method of claim 1, wherein disposing comprises disposing structures comprising gates each configured to store more than one bit per gate.

7.   The method of claim 1, wherein disposing comprises:

forming a first gate dielectric on the surface edge;

forming a floating gate on the first gate dielectric, wherein the floating gate is

configured to store more than one bit per floating gate;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

8.   The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures, wherein the structures providing the

electronic memory function are configured to store more than one bit per gate.

9.   The method of claim 1, wherein the semiconductor substrate comprises silicon.

10.   A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function spaced

apart a distance equal to one half of a minimum pitch of the array; and

establishing electrical contacts to memory cells including the non-horizontal

structures.

11.   The method of claim 10, further comprising:

incising the substrate to provide an array of substantially vertical edge surfaces, pairs

of the edge surfaces facing one another and spaced apart a distance equal to

one half of a minimum pitch of the array of edges; and

doping second regions between the pairs of edge surfaces, wherein:

disposing comprises disposing the non-horizontal structures on the substantially

vertical edge surfaces; and

establishing electrical contacts includes establishing electrical contacts to the first and

second regions and to the non-horizontal structures.

12. The method of claim 11, wherein disposing the non-horizontal structures on the

substantially vertical edge surfaces comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures, wherein the structures providing the

electronic memory function are configured to store more than one bit per gate.

13. The method of claim 11, wherein disposing the non-horizontal structures on the

substantially vertical edge surfaces comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures.

14. The method of claim 10, wherein the structures providing the electronic memory

function are configured to store more than one bit per gate.

15. The method of claim 11, wherein disposing non-horizontal structures comprises:

forming a first gate dielectric on the edge surfaces;

forming a floating gate on the first gate dielectric, wherein the floating gate is

configured to store more than one bit per floating gate;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

16. The method of claim 11, wherein disposing the non-horizontal structures on the

substantially vertical edge surfaces comprises:

forming a first gate dielectric on the surface edge;

forming a floating gate on the first gate dielectric;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

17.   The method of claim 11, wherein disposing comprises forming respective polysilicon gates on the edge surfaces.

18.   The method of claim 10, wherein disposing comprises forming respective polysilicon gates.

19.   The method of claim 10, wherein disposing comprises disposing a structure that is configured to provide an electronic memory function by storing holes.

20.   The method of claim 10, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

21.   A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function spaced apart a distance equal to one half of a minimum pitch of the array, wherein the structures providing the electronic memory function are configured to store more than one bit per gate; and

establishing electrical contacts to memory cells including the non-horizontal structures.

22.   The method of claim 21, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

23.   An array of memory cells configured to store at least one bit per one F^2 comprising:

memory cells arranged in rows and columns each coupled to respective row and column decoding circuitry, wherein each memory cell comprises:

first doped regions formed on a surface of a semiconductor substrate;

an array of incisions formed into the substrate to provide an array of substantially vertical edge surfaces, pairs of the edge surfaces facing one another and spaced apart a distance equal to one half of a pitch of the array of edge surfaces;

second doped regions formed between the pairs of edge surfaces;

respective structures each providing an electronic memory function disposed on at least some respective ones of the edge surfaces; and

electrical contacts to the first and second regions and to the structures providing the electronic memory function.

24. The array of claim 23, wherein the structures providing an electronic memory function each comprise:

ONO structures formed on at least some respective ones of the edge surfaces; and

respective gates formed on the ONO structures.

25. The array of claim 23, wherein the structures providing an electronic memory function each comprise:

ONO structures each formed on at least some respective ones of the edge surfaces; and

respective gates formed on the ONO structures, wherein the ONO structures comprise:

silicon dioxide grown from silicon comprising the edge surfaces;

silicon nitride formed on the silicon dioxide; and

silicon dioxide formed on the silicon nitride.

26. The array of claim 23, wherein the structures providing an electronic memory function each comprise respective polysilicon gates formed on respective ones of the surface edges.

27. The array of claim 23, wherein the structures providing an electronic memory function each comprise:

a first gate dielectric formed on the edge surfaces;

a floating gate formed on the first gate dielectric;

a second gate dielectric formed on the floating gate; and

a control gate formed on the second gate dielectric.

28. The array of claim 23, wherein the structures providing an electronic memory function each comprise structures each configured to store more than one bit per gate.

29. The array of claim 23, wherein the structures providing an electronic memory function each comprise:

a first gate dielectric formed on the edge surfaces;

a floating gate formed on the first gate dielectric, wherein the floating gate is configured to store more than one bit per floating gate;

a second gate dielectric formed on the floating gate; and

a control gate formed on the second gate dielectric.

30. The array of claim 23, wherein the structures providing an electronic memory function each comprise:

ONO structures formed on at least some of the edge surfaces; and

respective gates formed on the ONO structures, wherein the structures providing the electronic memory function are configured to store more than one bit per gate.

31. The array of claim 23, wherein the semiconductor substrate comprises silicon.

32. An array of memory cells configured to store at least one bit per one F^2 comprising:

memory cells arranged in rows and columns each coupled to respective row and column decoding circuitry, wherein each memory cell comprises:

substantially vertical structures providing an electronic memory function spaced apart a distance equal to one half of a minimum pitch of the array; and

electrical contacts to the memory cells including the substantially vertical structures.

33. The array of claim 32, further comprising:

incisions in the substrate that provide an array of substantially vertical edge surfaces,
pairs of the edge surfaces facing one another and spaced apart a distance equal
to one half of a minimum pitch of the array of edge surfaces; and

second doped regions formed between the pairs of edge surfaces, wherein:

the substantially vertical structures are formed on the substantially vertical edge
surfaces; and

the electrical contacts include electrical contacts to the first and second regions and to
the substantially vertical structures.

34. The array of claim 33, wherein the substantially vertical structures on the substantially
vertical edge surfaces each comprise:

ONO structures formed on at least some of the edge surfaces; and

respective gates formed on the ONO structures, wherein the structures providing the
electronic memory function are configured to store more than one bit per gate.

35. The array of claim 33, wherein disposing the substantially vertical structures on the
substantially vertical edge surfaces comprises:

ONO structures formed on at least some of the edge surfaces; and

respective gates formed on the ONO structures.

36. The array of claim 32, wherein the structures providing the electronic memory
function are configured to store more than one bit per gate.

37. The array of claim 33, wherein each substantially vertical structure comprises:

a first gate dielectric formed on the edge surfaces;

a floating gate formed on the first gate dielectric, wherein the floating gate is
configured to store more than one bit per floating gate;

a second gate dielectric formed on the floating gate; and

a control gate formed on the second gate dielectric.

38.   The array of claim 33, wherein each of the substantially vertical structures on the substantially vertical edge surfaces comprises:
        a first gate dielectric formed on the surface edge;
        a floating gate formed on the first gate dielectric;
        a second gate dielectric formed on the floating gate; and
        a control gate formed on the second gate dielectric.

39.   The array of claim 33, wherein the substantially vertical structures each include respective polysilicon gates formed on the edge surfaces.

40.   The array of claim 32, wherein the substantially vertical structures comprise respective polysilicon gates.

41.   The array of claim 32, wherein the substantially vertical structures are configured to provide an electronic memory function by storing holes.

42.   An array of memory cells configured to store at least one bit per one F^2 comprising:
        substantially vertical structures providing an electronic memory function spaced apart
                a distance equal to one half of a minimum pitch of the array, wherein the
                structures providing the electronic memory function are configured to store
                more than one bit per gate; and
        electrical contacts to the memory cells including the substantially vertical structures.

43.   A method of programming a memory cell in an array of memory cells configured to store at least one bit per F^2, comprising:
        coupling a first electrode to a first potential, where the first electrode is coupled to one
                of a first doped region disposed on a surface of a semiconductor substrate and
                a second doped region disposed on a bottom surface of one of a plurality of
                trenches formed in the substrate surface;
        coupling a second electrode to a second potential, where the second electrode is
                coupled to another of the first and second doped regions;

coupling a third electrode to a gate formed adjacent one of a plurality substantially vertical structures each providing electronic memory functions and that are spaced apart a distance equal to one half of a minimum pitch of the array on opposing sidewalls of the plurality of trenches between the first and second doped regions, wherein the structures providing the electronic memory functions are configured to store more than one bit per gate; and

storing charge carriers in the one substantially vertical structure.

44. The method of claim 43, wherein the substantially vertical structure comprises an ONO structure, the charge carriers comprise electrons and the charge carriers are stored at an edge of the ONO structure that is disposed adjacent one or the other of the first and second doped regions.

45. The method of claim 43, wherein the substantially vertical structure comprises an ONO structure and the charge carriers comprise electrons, and wherein the ONO structure is configured to be able to store charge at at least one of edges of the ONO structures that are disposed adjacent the first and second doped regions.

46. The method of claim 43, further comprising exposing the ONO structure to conditions effective to remove charge carriers stored in the ONO structure.

47. The method of claim 43, wherein storing charge carriers in the one substantially vertical structure comprises storing charge carriers at a first physical location in the one substantially vertical structure, and further comprising reversing the first and second potentials to store charge carriers at a second physical location within the one substantially vertical structure.

48. An array of memory cells configured to store at least one bit per one F^2 comprising: memory cells arranged in rows and columns each coupled to respective row and column decoding circuitry, wherein each memory cell comprises:

spaced-apart structures providing an electronic memory function separated by a
distance equal to one half of a minimum pitch of the array; and
electrical contacts to the memory cells including the spaced-apart structures.

49.   The array of claim 48, wherein the spaced apart structure comprise substantially
vertical structures.

50.   The array of claim 49, further comprising:
incisions in the substrate that provide an array of substantially vertical edge surfaces,
pairs of the edge surfaces facing one another and spaced apart a distance equal
to one half of a minimum pitch of the array of edge surfaces; and
second doped regions formed between the pairs of edge surfaces, wherein:
the substantially vertical structures are formed on the substantially vertical edge
surfaces; and
the electrical contacts include electrical contacts to the first and second regions and to
the substantially vertical structures.

51.   The array of claim 50, wherein the substantially vertical structures on the substantially
vertical edge surfaces each comprise:
ONO structures formed on at least some of the edge surfaces; and
respective gates formed on the ONO structures, wherein the structures providing the
electronic memory function are configured to store more than one bit per gate.

52.   A vertical multistate cell, comprising:
a vertical metal oxide semiconductor field effect transistor (MOSFET) extending
outwardly from a substrate, the MOSFET having a first source/drain region, a
second source/drain region, a channel region between the first and the second
source/drain regions, and a gate separated from the channel region by a gate
insulator;
a sourceline formed in a trench adjacent to the vertical MOSFET, wherein the first
source/drain region is coupled to the sourceline;

a transmission line coupled to the second source/drain region; and

wherein the MOSFET is a programmed MOSFET having one of a number of charge levels trapped in the gate insulator adjacent to the first source/drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed MOSFET operates at reduced drain source current.

53. The multistate cell of claim 52, wherein the first source/drain region of the MOSFET includes a source region and the second source/drain region of the MOSFET includes a drain region.

54. The multistate cell of claim 52, wherein the transmission line includes a bit line.

55. The multistate cell of claim 52, wherein the number of charge levels trapped in the gate insulator adjacent the first source/drain region includes a trapped electron charge.

56. The multistate cell of claim 52, wherein the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region.

57. The multistate cell of claim 56, wherein the Vt2 has a higher voltage threshold than the Vt1.

58. The multistate cell of claim 52, wherein the gate insulator has a thickness of approximately 10 nanometers (nm).

59. The multistate cell of claim 58, wherein the gate insulator includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and aluminum oxide (Al_2O_3).

60. A vertical multistate cell, comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate, the MOSFET having a source region, a drain region, a channel region between the source region and the drain region, and a gate separated from the channel region by a gate insulator;

a wordline coupled to the gate;

a sourceline formed in a trench adjacent to the vertical MOSFET, wherein the source region is coupled to the sourceline;

a bit line coupled to the drain region; and

wherein the MOSFET is a programmed MOSFET having a number of charge levels trapped in the gate insulator adjacent to the source region such that the channel region has a first voltage threshold region (Vt1) adjacent to the drain region and a second voltage threshold region (Vt2) adjacent to the source region, the Vt2 having a greater voltage threshold than Vt1.

61. The multistate cell of claim 60, wherein the gate insulator has a thickness of approximately 10 nanometers (nm).

62. The multistate cell of claim 61, wherein the gate insulator includes a gate insulator selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators.

63. The multistate cell of claim 60, wherein the gate insulator includes a composite layer.

64. The multistate cell of claim 63, wherein the composite layer includes a composite layer selected from the group of an oxide-aluminum oxide (Al_2O_3)-oxide composite layer, and oxide-silicon oxycarbide-oxide composite layer.

65.   The multistate cell of claim 63, wherein the composite layer includes a composite layer, or a non-stoichiometric single layer of two or more materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta).

66.   The multistate cell of claim 60, wherein the gate insulator includes a multiple layer of oxide-nitride-oxide (ONO).

67.   A memory array, comprising:

a number of vertical multistate cells extending from a substrate and separated by trenches, wherein each vertical multistate cell includes a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator;

a number of bit lines coupled to the second source/drain region of each multistate cell along rows of the memory array;

a number of word lines coupled to the gate of each multistate cell along columns of the memory array;

a number of sourcelines, wherein the first source/drain region of each vertical multistate cell is coupled to the number of sourcelines along rows in trenches between the number of vertical multistate cells extending from a substrate; and

wherein at least one of multistate cells is a programmed MOSFET having one of a number of charge levels trapped in the gate insulator adjacent to the first source/drain region such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed MOSFET operates at reduced drain source current.

68.   The memory array of claim 67, wherein the one of a number of charge levels trapped in the gate insulator includes a charge adjacent to the source of approximately 10 electrons.

69. The memory array of claim 67, wherein the first source/drain region of the MOSFET includes a source region and the second source/drain region of the MOSFET includes a drain region.

70. The memory array of claim 67, wherein the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region, and wherein Vt2 has a higher voltage threshold than the Vt1.

71. The memory array of claim 67, wherein the gate insulator of each multistate cell has a thickness of approximately 10 nanometers (nm).

72. The memory array of claim 71, wherein the gate insulator includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

73. The memory array of claim 71, wherein the number of vertical multistate cells extending from a substrate operate as equivalent to a transistor having a size of much less than 1.0 lithographic feature squared ($1F^2$).

74. A memory array, comprising:
   a number of vertical pillars formed in rows and columns extending outwardly from a substrate and separated by a number of trenches, wherein the number of vertical pillars serve as transistors including a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator in the trenches along rows of pillars, wherein along columns of the pillars adjacent pillars include a transistor which operates as a multistate cell on one side of a trench and a transistor which operates as a reference cell having a programmed conductivity state on the opposite side of the trench;

a number of bit lines coupled to the second source/drain region of each transistor along rows of the memory array;

a number of word lines coupled to the gate of each transistor along columns of the memory array;

a number of sourcelines formed in a bottom of the trenches between rows of the pillars and coupled to the first source/drain regions of each transistor along rows of pillars, wherein along columns of the pillars the first source/drain region of each transistor in column adjacent pillars couple to the sourceline in a shared trench such that a multistate cell transistor and a reference cell transistor share a common sourceline; and

wherein at least one of multistate cell transistors is a programmed MOSFET having one of a number of charge levels trapped in the gate insulator adjacent to the first source/drain region such that the channel region of that transistor has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed MOSFET operates at reduced drain source current.

75.   The memory array of claim 74, wherein the number of sourcelines formed in a bottom of the trenches between rows of the pillars include a doped region implanted in the bottom of the trench.

76.   The memory array of claim 74, wherein the one of a number of charge levels trapped in the gate insulator includes a charge adjacent to the source of approximately 10 electrons.

77.   The memory array of claim 74, wherein the second voltage threshold region (Vt2) in the channel is adjacent the first source/drain region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the second source/drain region, and wherein Vt2 has a higher voltage threshold than the Vt1.

78. The memory array of claim 74, wherein the gate insulator of each multistate cell transistor has a thickness of approximately 10 nanometers (nm).

79. The memory array of claim 78, wherein the gate insulator of each multistate cell transistor includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

80. The memory array of claim 74, wherein each multistate cell transistors operate as equivalent to a transistor having a size of much less than 1.0 lithographic feature squared ($1F^2$).

81. A memory device, comprising:
   a memory array, wherein the memory array includes a number of vertical multistate cells extending outwardly from a substrate and separated by trenches, wherein each multistate cell includes a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator;
   a number of bitlines coupled to the drain region of each vertical multistate cell along rows of the memory array;
   a number of wordlines coupled to the gate of each vertical multistate cell along columns of the memory array;
   a number of sourcelines, wherein the first source/drain region of each vertical multistate cell is coupled to the number of sourcelines along rows in trenches between the number of vertical multistate cells extending from a substrate;
   a wordline address decoder coupled to the number of wordlines;
   a bitline address decoder coupled to the number of bitlines;
   a sense amplifier coupled to the number of bitlines, wherein each sense amplifier is further coupled to a number of reference cells having a programmed conductivity state; and
   wherein at least one of multistate cells is a programmed MOSFET having a one or more charge levels trapped in the gate insulator adjacent to the source region

such that the channel region has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) and such that the programmed MOSFET operates at reduced drain/source current.

82.   The memory device of claim 81, wherein the one or more charge levels trapped in the gate insulator includes a charge adjacent to the source of approximately 10 electrons.

83.   The memory device of claim 81, wherein the second voltage threshold region (Vt2) in the channel is adjacent the source region, and wherein the first voltage threshold region (Vt1) in the channel is adjacent the drain region, and wherein Vt2 has a higher voltage threshold than the Vt1.

84.   The memory device of claim 83, wherein the gate insulator of each multistate cell transistor includes an oxide-nitride-oxide (ONO) insulator.

85.   The memory device of claim 84, wherein the gate insulator of each multistate cell has a thickness of approximately 10 nanometers (nm).

86.   The memory device of claim 81, wherein the wordline address decoder and the bitline address decoder each include conventionally fabricated MOSFET transistors having thin gate insulators formed of silicon dioxide (SiO_2).

87.   The memory device of claim 81, wherein the sense amplifier includes conventionally fabricated MOSFET transistors having thin gate insulators formed of silicon dioxide (SiO_2) .

88.   An electronic system, comprising:
a processor; and
a memory device coupled to the processor, wherein the memory device includes a memory array, the memory array including;

a number of vertical pillars formed in rows and columns extending outwardly
from a substrate and separated by a number of trenches, wherein the
number of vertical pillars serve as transistors including a first
source/drain region, a second source/drain region, a channel region
between the first and the second source/drain regions, and a gate
separated from the channel region by a gate insulator in the trenches
along rows of pillars, wherein along columns of the pillars adjacent
pillars include a transistor which operates as a multistate cell on one
side of a trench and a transistor which operates as a reference cell
having a programmed conductivity state on the opposite side of the
trench;

a number of bit lines coupled to the second source/drain region of each
transistor along rows of the memory array;

a number of word lines coupled to the gate of each transistor along columns of
the memory array;

a number of sourcelines formed in a bottom of the trenches between rows of
the pillars and coupled to the first source/drain regions of each
transistor along rows of pillars, wherein along columns of the pillars
the first source/drain region of each transistor in column adjacent
pillars couple to the sourceline in a shared trench such that a multistate
cell transistor and a reference cell transistor share a common
sourceline; and

wherein at least one of multistate cell transistors is a programmed MOSFET
having one of a number of charge levels trapped in the gate insulator
adjacent to the first source/drain region such that the channel region of
that transistor has a first voltage threshold region (Vt1) and a second
voltage threshold region (Vt2) and such that the programmed MOSFET
operates at reduced drain source current.

89.   The electronic system of claim 88, wherein the one of the number of charge levels
trapped in the gate insulator includes a charge of approximately 10 electrons.

90. The electronic system of claim 88, wherein the gate insulator of each multistate cell transistor includes a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

91. The electronic system of claim 88, wherein the gate insulator of each multistate cell transistor includes an oxide-nitride-oxide (ONO) insulator.

92. The electronic system of claim 88, wherein each multistate cell transistors operate as equivalent to a transistor having a size of much less than 1.0 lithographic feature squared ($1F^2$).

93. The electronic system of claim 88, wherein, in a read operation, a sourceline for two column adjacent pillars sharing a trench is coupled to a ground potential, the drain regions of the column adjacent pillars sharing a trench are precharged to a fractional voltage of VDD, and the gate for each of the column adjacent pillars sharing a trench is addressed such that a conductivity state of a multistate cell memory cell transistor can be compared to a conductivity state of a reference cell.

94. The electronic system of claim 88, wherein, in a write operation, a sourceline for two column adjacent pillars sharing a trench is biased to a voltage higher than VDD, one of the drain regions of the column adjacent pillars sharing a trench is coupled to a ground potential, and the gate for each of the column adjacent pillars sharing a trench is addressed with a wordline potential.

95. A method for operating a memory, comprising:
    programming one or more vertical MOSFETs extending outwardly from a substrate
        and separated by trenches in a DRAM array in a reverse direction, wherein
        each MOSFET in the DRAM array includes a source region, a drain region, a
        channel region between the source and the drain regions, and a gate separated
        from the channel region by a gate insulator in the trenches, wherein the DRAM

array includes a number of sourcelines formed in a bottom of the trenches between rows of the vertical MOSFETs and coupled to the source regions of each transistor along rows the vertical MOSFETs, wherein along columns of the vertical MOSFETs the source region of each column adjacent vertical MOSFET couple to the sourceline in a shared trench, and wherein the DRAM array includes a number of bitlines coupled to the drain region along rows in the DRAM array, and wherein programming the one or more vertical MOSFETs in the reverse direction includes:

applying a first voltage potential to a drain region of the vertical MOSFET;

applying a second voltage potential to a source region of the vertical
    MOSFET;

applying a gate potential to a gate of the vertical MOSFET; and

wherein applying the first, second and gate potentials to the one or more vertical MOSFETs includes creating a hot electron injection into the gate insulator of the one or more MOSFETs adjacent to the source region such that the one or more vertical MOSFETs become programmed MOSFETs having one of a number of charge levels trapped in the gate insulator such that the programmed MOSFET operates at reduced drain source current in a forward direction.

96.   The method of claim 95, wherein applying a first voltage potential to the drain region of the vertical MOSFET includes grounding the drain region of the vertical MOSFET.

97.   The method of claim 95, wherein applying a second voltage potential to the source region includes applying a high voltage potential (VDD) to a sourceline coupled thereto.

98.   The method of claim 95, wherein applying a gate potential to the gate of the vertical MOSFET includes applying a gate potential to the gate in order to create a conduction channel between the source and drain regions of the vertical MOSFET.

99.   The method of claim 95, wherein the method further includes reading one or more vertical MOSFETs in the DRAM array by operating an addressed vertical MOSFET in a forward direction, wherein operating the vertical MOSFET in the forward direction includes:

grounding a sourceline for two column adjacent pillars sharing a trench;

precharging the drain regions of the column adjacent pillars sharing a trench to a fractional voltage of VDD; and

applying a gate potential of approximately 1.0 Volt to the gate for each of the column adjacent pillars sharing a trench such that a conductivity state of the addressed vertical MOSFET can be compared to a conductivity state of a reference cell.

100.   The method of claim 95, wherein in creating a hot electron injection into the gate insulator of the one or more vertical MOSFETs adjacent to the source region includes creating a first threshold voltage region (Vt1) adjacent to the drain region and creating a second threshold voltage region (Vt2) adjacent to the source region.

101.   The method of claim 95, wherein in creating a hot electron injection into the gate insulator of the one or more vertical MOSFETs adjacent to the source region includes changing a threshold voltage for the vertical MOSFET adjacent to the source by approximately 0.16 Volts.

102.   A method for multistate memory, comprising:

writing to one or more vertical MOSFETs arranged in rows and columns extending outwardly from a substrate and separated by trenches in a DRAM array in a reverse direction, wherein each MOSFET in the DRAM array includes a source region, a drain region, a channel region between the source and the drain regions, and a gate separated from the channel region by a gate insulator in the trenches, wherein the DRAM array includes a number of sourcelines formed in a bottom of the trenches between rows of the vertical MOSFETs and coupled to the source regions of each transistor along rows the vertical MOSFETs, wherein along columns of the vertical MOSFETs the source region

of each column adjacent vertical MOSFET couple to the sourceline in a shared trench, and wherein the DRAM array includes a number of bitlines coupled to the drain region along rows in the DRAM array, and wherein programming the one or more vertical MOSFETs in the reverse direction includes;

biasing a sourceline for two column adjacent vertical MOSFETs sharing a trench to a voltage higher than VDD;

grounding a bitline coupled to one of the drain regions of the two column adjacent vertical MOSFETs in the vertical MOSFET to be programmed

applying a gate potential to the gate for each of the two column adjacent vertical MOSFETs to create a hot electron injection into the gate insulator of the vertical MOSFET to be programmed adjacent to the source region such that the addressed MOSFETs becomes a programmed MOSFET and will operate at reduced drain source current in a forward direction;

reading one or more vertical MOSFETs in the DRAM array in a forward direction, wherein reading the one or more MOSFETs in the forward direction includes;

grounding a sourceline for two column vertical MOSFETs sharing a trench;

precharging the drain regions of the two column adjacent vertical MOSFETs sharing a trench to a fractional voltage of VDD; and

applying a gate potential of approximately 1.0 Volt to the gate for each of the two column adjacent vertical MOSFETs sharing a trench such that a conductivity state of an addressed vertical MOSFET can be compared to a conductivity state of a reference cell.

103. The method of claim 102, wherein in creating a hot electron injection into the gate insulator of the addressed MOSFET adjacent to the source region includes creating a first threshold voltage region (Vt1) adjacent to the drain region and creating a second threshold voltage region (Vt2) adjacent to the source region, wherein Vt2 is greater that Vt1.

104.   The method of claim 102, wherein in creating a hot electron injection into the gate insulator of the addressed MOSFET adjacent to the source region includes changing a threshold voltage for the MOSFET adjacent to the source by approximately 0.16 Volts.

105.   The method of claim 102, wherein in creating a hot electron injection into the gate insulator of the addressed MOSFET adjacent to the source region includes trapping a stored charge in the gate insulator of the addressed MOSFET adjacent to the source of approximately 10 electrons.

106.   The method of claim 102, wherein reading the one or more MOSFETs in the forward direction includes using a sense amplifier to detect whether an addressed MOSFET is a programmed MOSFET, wherein a programmed MOSFET will exhibit a change in an integrated drain current of approximately 4.0 μA when addressed over approximately 10 ns.

107.   A method for forming a multistate memory array, comprising:
          forming a number of vertical pillars in rows and columns extending outwardly from a substrate and separated by a number of trenches, wherein the number of vertical pillars serve as transistors including a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel region by a gate insulator in the trenches along rows of pillars, wherein along columns of the pillars adjacent pillars include a transistor which operates as a multistate cell on one side of a trench and a transistor which operates as a reference cell having a programmed conductivity state on the opposite side of the trench;
          forming a number of bit lines coupled to the second source/drain region of each transistor along rows of the memory array;
          forming a number of word lines coupled to the gate of each transistor along columns of the memory array;

forming a number of sourcelines formed in a bottom of the trenches between rows of the pillars and coupled to the first source/drain regions of each transistor along rows of pillars, wherein along columns of the pillars the first source/drain region of each transistor in column adjacent pillars couple to the sourceline in a shared trench such that a multistate cell transistor and a reference cell transistor share a common sourceline; and

wherein the number of vertical pillars can be programmed in a reverse direction to have a one of a number of charge levels trapped in the gate insulator adjacent to the first source/drain region by biasing a sourceline to a voltage higher than VDD, grounding a bitline, and selecting a gate by a wordline address.

108. The method of claim 107, wherein forming a number of sourcelines formed in a bottom of the trenches between rows of the pillars includes implanting a doped region in the bottom of the trench.

109. The method of claim 107, wherein, in forming a gate insulator above the channel region in the trenches along rows of pillars, the method includes forming a gate insulator having a thickness of at least 10 nanometers (nm).

110. The method of claim 107, wherein, in forming a gate insulator above the channel region in the trenches along rows of pillars, the method includes forming a gate insulator selected from the group of silicon dioxide (SiO_2) formed by wet oxidation, silicon oxynitride (SON), and silicon rich aluminum oxide.

111. The method of claim 107, wherein, in forming a gate insulator above the channel region in the trenches along rows of pillars, the method includes forming an oxide-nitride-oxide (ONO) insulator.

112. The method of claim 107, wherein forming a number of vertical pillars in rows and columns extending outwardly from a substrate and separated by a number of trenches, wherein the number of vertical pillars serve as transistors includes forming a number

of vertical pillars having a storage density which is much greater than one bit for each 1.0 lithographic feature squared ($1F^2$) unit area.